What is claimed is:

1. A digital multiplication apparatus adopting a redundant binary arithmetic for multiplying two numbers X and Y using a radix-2k number system, the apparatus comprising:

a data converter for data-converting the m-bit number Y into m/k-digit data D ($= D_{m/k-1}D_{m/k-2} \ldots. D_i \ldots D_iD_0$);

a partial product calculator for converting each of the digits Di of the number Y converted by the data converter into a combination of the coefficients of a fundamental multiple, multiplying the combination by the number X, and outputting the product as a redundant binary partial product;

a redundant binary adder for summing the partial products for all of the digits of the converted number Y; and

a redundant binary (RB)-normal binary (NB) converter for converting the redundant binary sum into a normal binary number and outputting the converted normal binary sum as the product of the two numbers.

2. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 1, wherein the partial product calculator comprises:

a fundamental multiple determiner for dividing the number Y into upper bits and lower bits by recoding the number Y, determining the sum of the products of the divided lower bits by corresponding weighted values to be the coefficient of the fundamental multiple, determining the product of the sum of the products of the divided upper bits by corresponding weighted values by 2^k to be the coefficient of the fundamental multiple, and multiplying the determined coefficients of the fundamental multiple by the number X and outputting the product as the fundamental multiple;

first through m/k-th multiplexers;

first through m/k-th logic combination units; and

a controller for receiving all of the digits of the number Y converted by the data converter, producing the combination of the coefficients of the fundamental multiple with respect to each digit D_i, and generating selection signals according to the produced combination,

wherein each of the multiplexers selects two among the fundamental multiples in response to the selection signals, and the logic combination units perform logic combinations on the fundamental multiples selected by the multiplexers and output the results of the logic combinations as the redundant binary partial products to the RB-NB converter.

3. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 2, wherein each of the logic combination units comprises:

a first inverter for inverting one of the two selected fundamental multiples;

a second inverter for inverting the other fundamental multiple;

a first exclusive OR unit for performing an exclusive OR operation on the output of the first inverter and an n-th bit from the least significant bit of the number Y; and

a second exclusive OR unit for performing an exclusive OR operation on the output of the second inverter and the most significant bit of the number Y,

wherein the results of the exclusive OR operations by the first and second exclusive OR units are the redundant binary partial products.

4. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 3, wherein each of the logic combination units further comprises:

a first inversion OR unit for performing an inversion OR operation on the outputs of the first and second exclusive OR units;

a first AND unit for performing an AND operation on the outputs of the first and second exclusive OR units; and

a second inversion OR unit for performing an inversion OR operation on the output of the first AND unit and the output of the first inversion OR unit.

5. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 3, wherein the redundant binary adder comprises first through $\log_2(\left\lceil \frac{m}{k}+1 \right\rceil)$ redundant binary adding ports, each of the redundant binary adding ports has a predetermined number of adders, each of the adders adds two

redundant binary partial products (a_i^+, a_i^-) and (b_i^+, b_i^-) using the following logic combination formula to obtain (d_i^+, d_i^-):

$$
\begin{aligned}
d_i^+ &= (l_i \oplus h_{i-1}) \cdot (\overline{l_{i-1}} \cdot k_{i-1} + l_{i-1} \cdot h_{i-2}) \equiv \alpha_i \cdot \overline{\beta_{i-1}} \\
d_i^- &= \overline{(l_i \oplus h_{i-1})} \cdot (\overline{l_{i-1}} \cdot \overline{k_{i-1}} + l_{i-1} \cdot \overline{h_{i-2}}) \equiv \overline{\alpha_i} \cdot \beta_{i-1}
\end{aligned}
$$

$$
\left(
\begin{aligned}
&here,\ l_i = (a_i^+ \oplus a_i^-) \oplus (b_i^+ \oplus b_i^-) \\
&h_i = a_i^+ \cdot \overline{a_i^-} + b_i^+ \cdot \overline{b_i^-} \\
&k_i = \overline{(a_i^+ \oplus a_i^-)} + (a_i^+ \cdot \overline{a_i^-}) + (b_i^+ \cdot \overline{b_i^-})
\end{aligned}
\right)
$$

6. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 5, wherein each of the adders comprises:

a third inversion OR unit for performing an inversion OR operation on the output of the second inversion OR unit of the corresponding logic combination unit and a previous carry parameter h_{i-1};

a second AND unit for performing an AND operation on the output of the second inversion OR unit of the corresponding logic combination unit and the previous carry parameter h_{i-1};

a fourth inversion OR unit for performing an inversion OR operation on the output of the third inversion OR unit and the output of the second AND unit;

a fifth inversion OR unit for performing an inversion OR operation on the result of the previous inversion OR operation by the third inversion OR unit and the output of the fourth inversion OR unit;

a third AND unit for performing an AND operation on the result of the previous inversion OR operation by the third inversion OR unit and the output of the fourth inversion OR unit; and

a sixth inversion OR unit for performing an inversion OR operation on the output of the fifth inversion OR unit and the output of the third AND unit,

wherein the output of the fifth inversion OR unit is $d_i^+ \cdot \overline{d_i^-}$, and the output of the sixth inversion OR unit is $\overline{d_i^+ \oplus d_i^-}$.

7. The digital multiplication apparatus adopting a redundant binary arithmetic of claim 5, wherein each of the adders comprises:

a fourth AND unit for performing an AND operation on the output of the first inversion OR unit of a logic combination unit and the output of the first inversion OR unit of another logic combination unit;

a seventh inversion OR unit for performing an inversion OR operation on the inputs of the fourth AND unit;

an eighth inversion OR unit for performing an inversion OR operation on the output of the fourth AND unit and the output of the second inversion OR unit of the former logic combination unit;

a third inverter for inverting the output of the second inversion OR unit of the former logic combination unit;

a complementary MOS inverter installed between the output of the second inversion OR unit of the former logic combination unit and the output of the third inverter, for receiving and inverting the output of the second inversion OR unit of the latter logic combination unit;

a fourth inverter for inverting the output of the complementary MOS inverter;

a first transmission gate for transmitting the input of the complementary MOS inverter to the fourth inverter in response to the output of the second inversion OR unit of the former logic combination unit and the output of the third inverter;

a fifth inverter for inverting the previous output of the seventh inversion OR unit;

a second transmission gate for transmitting the output of the fifth inverter in response to the output of the fourth inverter and the output of the complementary MOS inverter;

a third transmission gate for transmitting the previous output of the seventh inversion OR unit in response to the output of the complementary MOS inverter and the output of the fourth inverter;

a fourth transmission gate for transmitting the previous output of the seventh inversion OR unit in response to the output of the fourth inverter and the output of the complementary MOS inverter;

a fifth transmission gate for transmitting the output of the eighth inversion OR unit in response to the output of the complementary MOS inverter and the output of the fourth inverter;

a ninth inversion OR unit for performing an inversion OR operation on the outputs of the second and third transmission gates and the previous outputs of the fourth and fifth transmission gates;

a fifth AND unit for performing an AND operation on the inputs of the ninth inversion OR unit; and

a tenth inversion OR unit for performing an inversion OR operation on the output of the fifth AND unit and the output of the ninth inversion OR unit,

wherein the output of the ninth inversion OR unit is $d_i^+ \cdot \overline{d_i^-}$, and the output of the tenth inversion OR unit is $\overline{d_i^+ \oplus d_i^-}$.

8. A digital multiplication method adopting a redundant binary arithmetic for multiplying two numbers X and Y using a radix-2k number system, the method comprising:

(a) data-converting the m-bit number Y into m/k-digit data D (= $D_{m/k-1}D_{m/k-2}$ .... D_i ... D_1D_0);

(b) converting each of the digits Di of the number Y into a combination of the coefficients of a fundamental multiple, and multiplying the combination by the number X to obtain a redundant binary partial product;

(c) summing the partial products for all of the digits of the number Y converted; and

(d) converting the redundant binary sum into a normal binary number to obtain the product of the two numbers.

9. The digital multiplication method adopting a redundant binary arithmetic of claim 8, wherein the step (b) comprises:

(b1) determining the coefficients of the fundamental multiple;

(b2) converting the data Di into a combination of the coefficients of the fundamental multiple; and

(b3) obtaining the redundant binary partial products by multiplying each of the combinations by the number X.

10. The digital multiplication method adopting a redundant binary arithmetic of claim 9, wherein the step (b1) comprises:

grouping the m bits of the number Y by consecutive (k+1) bits while consecutive groups overlap by one bit such that the last bit of each group is the first bit of the following group;

classifying the k bits excluding the most significant bit in the (k+1)- bit group into t upper bits and s ($\geq$t) lower bits;

obtaining an s-bit group value by multiplying each of the s lower bits by a corresponding weighted value among a predetermined number of weighted values and summing the products; and

obtaining a t-bit group value by multiplying each of the t upper bits by a corresponding weighted value among the predetermined number of weighted values, summing the products, and multiplying the sum by 2^s,

wherein the coefficients of the fundamental multiple are determined from the s-bit group values and the t-bit group values.

11. The digital multiplication method adopting a redundant binary arithmetic of claim 10, wherein, when k is 6, the corresponding weighted values are 1, 1 and 2, and the fundamental multiple coefficients are 0, 1, 2, 3, 4, 8, 16, 24 and 32.

12. The digital multiplication method adopting a redundant binary arithmetic of claim 9, wherein the step (b1) comprises:

(b11) initializing a decimal value s_grp_{10} of an s-bit binary number s_grp_2, when the number of lower bits of Y_j, which is a group of consecutive (k+1) bits grouped from the m bits of the number Y while consecutive groups overlap by one

bit such that the last bit of each group is the first bit of the following group, is s (where s is k-t, and t is $\left\lfloor \frac{k}{2} \right\rfloor$ (where $\lfloor x \rfloor$ denotes an integer that is x or the largest one among integers that are smaller than x);

(b12) obtaining the coefficient of the fundamental multiple as in the following Equation:

$$FMC[s\_grp_{10}] = s\_grp_2[0] + \sum_{j=1}^{s-1} s\_grp_2[j] * 2^{j-1}$$

wherein $s\_grp_2[i]$ denotes the i-th bit of s_grp_2;

(b13) determining whether s_grp_{10} is smaller than 2^s;

(b14) increasing s_grp_{10} by 1 and repeating the step (b12), if s_grp_{10} is smaller than 2^s;

(b15) initializing a decimal value t_grp_{10} of a binary number t_grp_2 composed of the t upper bits of Y_j, if s_grp_{10} is not smaller than 2^s;

(b16) obtaining the coefficient of a fundamental multiple as in the following Equation:

$$FMC[s\_grp_{10} + t\_grp_{10}] = 2^s * (t\_grp_2[0] + \sum_{j=1}^{t-1} t\_grp_2[j] * 2^{j-1})$$

wherein $t\_grp_2[i]$ denotes the i-th bit of t_grp_2;

(b17) determining whether t_grp_{10} is smaller than 2^t, and, if t_grp_{10} is not smaller than 2^t, repeating the step (b2); and

(b18) increases t_grp_{10} by 1 and repeating the step (b16), if t_grp_{10} is smaller than 2^t.